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EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,889	WEBER ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,21-28,35-38 and 49-52* is/are pending in the application.

4a) Of the above claim(s) *10-20,29-34, and 39-48, and 53-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,21-28,35-38 and 49-52* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03/03, 10/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on March 28, 2005, of Application No. 09/870889.

Claim Objections

2. Claim 2 is objected to because of the following informalities:

In line 1, the acronym "LPC" must be properly defined since it is its first usage in the claim.

Appropriate correction is required.

Information Disclosure Statement

3. The information disclosure statement filed 10/03/2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. Document titled "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for commercial Application" by Standard Microsystems Corporation, has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In the claim, Applicant discloses "bit 2 as the first read lock bit" and "bit 6 as the first read lock bit". This limitation is not enabling because the function and/or operation of those two bits would have been conflicted. For instance, when the "first read lock bit" tries to access a memory block, both bit 2 and bit 6 would be fighting to decide which one really access that memory block which can also result in a conflict of resources. It appears that at line 3, "bit 6 as the first read lock bit" should be changed to –bit 6 as the second read lock bit--.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 6, 21-25, 35-38, and 49-52, are rejected under 35 U.S.C. 102(b) as being anticipated by Hotley (5,442,704).

As per claim 1, Hotley discloses a computer system [*computer systems*; Fig.1, col.1, lines 21-22], comprising a bus [*a bus*; Fig.1, *bus 102*, col.2, line 65]; a memory coupled to the bus, wherein the memory includes a plurality of storage locations, wherein the plurality of storage locations are divided into a plurality of memory units [*a memory connect to the bus*; col.2, lines 64-65; *the memory is organized into a number of blocks, each block having a number of rows, each containing a plurality of locations*; col.3, lines 5-7]; and a device coupled to access the memory over the bus, wherein the device includes one or more locks configured to control access to one or more of the plurality of memory units [*each row includes lock bit location; the lock bits ensure data protection*; col.3, lines 7-14; *each memory device includes security control logic circuits which include access control memory having a plurality of access control storage elements and a programmable security access control unit containing circuits for carrying out a key validation operation*; Fig.2; col.3, lines 15-21].

As per claim 3, Hotley discloses the memory is a ROM [*the memory is a ROM*; col.5, lines 49-50].

As per claim 6, Hotley discloses the locks include a plurality of registers, wherein one or more entries in one or more of the plurality of registers indicate an access control setting for one or more of the memory units [*a first register, a second register, a third register*; col.8, lines 62-68; *lock bits ensure data protection*; col.3, lines 10-14].

As per claims 21, 35, and 49, Hotley discloses a method for operating a computer system, the method comprising: requesting a memory transaction for one or

more memory addresses [*transmitting address, data and control information*; col.2, lines 65-66; *transfer address, data and control information*; col.3, lines 2-3]; determining a lock status for the one or more memory addresses [*a status register 58 is used for storing the status*; col.7, lines 65-66; *the lock write enable flip-flop is in the set state, it causes the bit to be written into the designated first lock bit location of a memory block, in this the MSBs of the address are not loaded into the address register*; col.15, lines 62-66]; returning the lock status for the one or more memory addresses [*write bits of corresponding ones of the key values into the groups of lock bit locations of all the blocks designated as protected*; col.20, lines 25-27]; determining if the lock status for the one or more memory addresses can be changed if the lock status indicates that the memory transaction for the one or more memory addresses is not allowed [*allow the first bit in each group of lock bit locations of each block which is to be protected to be set; these elements cannot be changed*; col.10, lines 67-68, and col.11, lines 1-3]; changing the lock status of the one or more memory addresses to allow the memory transaction if the lock status of the one or more memory addresses can be changed [*the middle address bits stored in the address latch counter 30-3 to be incremented by one for readout of the next lock bit location LMB1; compared with the key bit presented, if both compare identically, then no action is taken to change the state*; col.13, lines 25-31].

As per claims 22, 36, and 50, Hotley discloses determining a lock status includes reading a first lock bit [*reading a next lock bit from the block's lock bit locations*; col.9, lines 63-64]; and wherein returning the lock status includes returning the value of the first lock bit [*the first bit of every key value is set to a predetermined state*; col.4, lines 4-5].

As per claims 23, 37, and 51, Hotley discloses determining if the lock status for the one or more memory address can be changed includes reading a second lock bit [*reading a next lock bit from the block's lock bit locations*; col.9, lines 63-64].

As per claims 24, 38, and 52, Hotley discloses changing the lock status of the one or more memory addresses to allow the memory transaction includes changing the value of the first lock bit [*the first bit of every key value is set to a predetermined state*; col.4, lines 4-5].

As per claim 25, Hotley discloses a method of operating a computer system [*a method of operating a computer system*; col.5, lines 40-41]; issuing a request from a first device for a memory transaction for a memory location [*compare data bit to the lock bit stored in a corresponding one of the lock bit locations*; col.3, lines 54-56]; receiving the request for the memory transaction at a second device that does not include the memory location or a copy of the contents of the memory location [*access control memory having a plurality of access control storage elements*; col.3, lines 17-18]; returning a response from the second device to the first device issuing the request for the memory transaction [*after successful performance of the validation operation, memory access control of a block is set for enabling the user to read out information from the protected block*; col.3, lines 30-34].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4, 7-8, and 26-27, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (5,442,704) in view of Gafken (6,026,016).

As per claim 4, Hotley discloses the claimed invention as discussed above in the previous paragraphs. However, Hotley does not specifically teach the ROM is a BIOS ROM as recited in the claim.

Gafken discloses the ROM is a BIOS ROM [the ROM is a BIOS ROM; col.1, lines 20-21] to store the startup and/or basic input/output system routines (col.1, lines 20-22).

Since the technology for implementing a memory system with the ROM being a BIOS ROM was well known as evidenced by Gafken, and since the ROM being a BIOS ROM stores the startup and/or basic input/output system routines, an artisan would have been motivated to implement this feature in the system of Hotley. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant to modify the system of Hotley to incorporate the ROM being a BIOS ROM

because it was well known to store the startup and/or basic input/output system routines (col.1, lines 20-22) as taught by Gafken.

As per claim 7, Hotley discloses at least one of the plurality of registers is configured to store three locking bits for one of the memory blocks, wherein the three locking bits include a read lock bit, a write lock bit [*a number of lock bits for each block*; col.3, lines 10-11; *lock bit read out from lock bit section 54a*; col.9, lines 15-16; *the bits of a key value can be used to cause the writing of the key value bit sequence into the lock bit*; col.4, lines 54-57].

However, Hotley does not specifically teach a lock-down bit, wherein the read lock bit and the write lock bit are permanent until reset when the lock-down bit is set as recited in the claim.

Gafken discloses a lock-down bit, wherein the read lock bit and the write lock bit are permanent until reset when the lock-down bit is set [*a lock- down bit*; Fig.4, col.5, lines 54-56; *the read lock bits may be reset or cleared; a lock bit array 705 includes a write lock bit, lock down bits, and a read lock bit*; Fig.7, col.8, lines 21-29; *determine whether write and read operations can proceed based on whether the corresponding lock down bit(s) are set*; col.8, lines 36-39] to provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory (col.1, lines 8-10).

Since the technology for implementing a memory system with a read lock bit, a write lock bit, and a lock-down bit was well known as evidenced by Gafken, and since a read lock bit, a write lock bit, and a lock-down bit provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory, an artisan would have been motivated to implement this feature in the system of Hotley. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant to modify the system of Hotley to incorporate a read lock bit, a write lock bit, and a lock-down bit, because it was well known to provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory (col.1, lines 8-10) as taught by Gafken.

As per claim 8, Hotley discloses at least one of the plurality of registers is configured to store eight bits [Fig.3, *Registers 55, 58*]; the eight bits include three locking bits for one of the memory blocks and another three locking bits for another one of the memory blocks [*a number of lock bits for each block*; col.3, lines 10-11; *lock bit read out from lock bit section 54a*; col.9, lines 15-16; *the bits of a key value can be used to cause the writing of the key value bit sequence into the lock bit*; col.4, lines 54-57].

However, Hotley does not specifically teach the three locking bits include a first read lock bit, a first write lock bit, and a first lock-down bit wherein when the first lock-down bit is set, the first read lock bit and the first write lock bit are permanent until reset, and wherein the another three locking bits include a second read lock bit, a second

write lock bit, and a second lock-down bit, wherein when the second lock-down bit is set, the second read lock bit and the second write lock bit are permanent until reset as recited in the claim.

Gafken discloses the three locking bits include a first read lock bit, a first write lock bit, and a first lock-down bit wherein when the first lock-down bit is set, the first read lock bit and the first write lock bit are permanent until reset, and wherein the another three locking bits include a second read lock bit, a second write lock bit, and a second lock-down bit, wherein when the second lock-down bit is set, the second read lock bit and the second write lock bit are permanent until reset [*a lock- down bit*; Fig.4, col.5, lines 54-56; *the read lock bits may be reset or cleared; a lock bit array 705 includes a write lock bit, lock down bits, and a read lock bit*; Fig.7, col.8, lines 21-29; *determine whether write and read operations can proceed based on whether the corresponding lock down bit(s) are set*; col.8, lines 36-39; *a read lock bit, a write lock bit, and a lock-down bit can be duplicated into a first and/or second read and/or write and/or lock-down bit*] to provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory (col.1, lines 8-10).

Since the technology for implementing a memory system with a read lock bit, a write lock bit, and a lock-down bit was well known as evidenced by Gafken, and since a read lock bit, a write lock bit, and a lock-down bit provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of

memory, an artisan would have been motivated to implement this feature in the system of Hotley. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant to modify the system of Hotley to incorporate a read lock bit, a write lock bit, and a lock-down bit, because it was well known to provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory (col.1, lines 8-10) as taught by Gafken.

As per claim 26, Hotley discloses the claimed invention as discussed above in the previous paragraphs. However, Hotley does not specifically teach returning the response from the second device includes ending the memory transaction without the memory transaction reaching the memory location as recited in the claim.

Gafken discloses returning the response from the second device includes ending the memory transaction without the memory transaction reaching the memory location [*if the block of memory cells is locked down, it can be unlocked to enable write and erase operations to the block of memory cells in response to the detection of a system reset*; col.3, lines 9-11; *the system reset ends the memory transaction without the memory transaction reaching the memory location*] to provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory (col.1, lines 8-10).

Since the technology for implementing a memory system where returning the response from the second device includes ending the memory transaction without the

memory transaction reaching the memory location was well known as evidenced by Gafken, and since returning the response from the second device includes ending the memory transaction without the memory transaction reaching the memory location provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory, an artisan would have been motivated to implement this feature in the system of Hotley. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant to modify the system of Hotley to incorporate ending the memory transaction without the memory transaction reaching the memory location, because it was well known to provide locking and unlocking of memory cells, disable and enable write and erase, and read operations to the blocks of memory (col.1, lines 8-10) as taught by Gafken.

As per claim 27, Gafken discloses ending the request for the memory transaction without the memory location responding to the request for the memory transaction [*if the block of memory cells is locked down, it can be unlocked to enable write and erase operations to the block of memory cells in response to the detection of a system reset*; col.3, lines 9-11; *the system reset ends the request without the memory location responding to the request*].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2, 5, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (5,442,704) in view of Watts, Jr. (6,816,925).

As per claim 2, Hotley discloses the claimed invention as discussed above in the previous paragraphs. However, Hotley does not specifically teach the bus is configured to operate according to an LPC bus protocol as recited in the claim.

Watts, Jr. discloses the bus is configured to operate according to an LPC bus protocol [LPC bus 305; Fig.3] to allow access to communication cards (col.4, lines 57-58).

Since the technology for implementing a memory system with LPC bus was well known as evidenced by Watts Jr., and since an LPC bus allows access to communication cards, an artisan would have been motivated to implement this feature in the system of Hotley. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant to modify the system of Hotley to incorporate an LPC bus because it was well known to allow access to communication cards (col.4, lines 57-58) as taught by Watts Jr..

As per claim 5, Hotley discloses the claimed invention as discussed above in the previous paragraphs. However, Hotley does not specifically teach the device is a south bridge as recited in the claim.

Watts Jr. discloses the device is a south bridge [Fig.3, south bridge] to allow access to communication cards (col.4, lines 57-58).

Since the technology for implementing a memory system with the device being a south bridge was well known as evidenced by Watts Jr., and since a south bridge allows access to communication cards, an artisan would have been motivated to implement this feature in the system of Hotley. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made by applicant to modify the system of Hotley to incorporate a south bridge because it was well known to allow access to communication cards (col.4, lines 57-58) as taught by Watts Jr..

As per claim 28, Watts Jr. discloses the second device includes a bridge coupled between the first device and the memory location, wherein said returning the response from the second device to the first device issuing the request for the memory transaction includes returning the response from the bridge to the first device issuing the request for the memory transaction [Fig.1, bridge 105, memory 130, CPU 100].

Reason for Indicating Allowable Subject Matter

11. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and also if rewritten or amended to overcome the 112 rejection.

12. The following is an examiner's statement of reasons for indicating allowable subject matter:

The closest prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

In combination with all the limitations of the claims, the prior art made of record fail to suggest or render obvious, in light of the specification and the drawings, the features of:

"at least one plurality of registers is configured with bit 0 as the first write lock bit, bit 1 as the first lock-down bit, bit 2 as the first read lock bit, bit 4 as the second write lock bit, bit 5 as the second lock-down bit, and bit 6 as the second read lock bit " of claim 15.

Therefore, when taken as a whole and read in light of the specification, the limitations of claim 9 are not taught or suggested by the prior art of record, taken alone or in combination.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamaki et al.	5,963,738
Abudayyeh et al.	5,796,981
Pearce et al.	5,896,534
Yamazaki et al.	6,038,632

14. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

15. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 25, 2005

M C

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